Remarks:

Reconsideration of the application is requested.

Claims 1 and 7-22 are now in the application. Claims 1, 7, 14-15 and 20 have been amended. Claims 21-22 have been added. Claim 6 has been cancelled.

In item 3 on page 2 of the above-mentioned Office action, claims 1 and 6-20 have been rejected as being anticipated by Cook et al. (US Pat. No. 6,300,785 B1) under 35 U.S.C. § 102(e).

The rejection has been noted and claims 1 and 20 have been amended in an effort to even more clearly define the invention of the instant application. More specifically, the feature of claim 6 has been added to claim 1. Amended claim 1 now recites the embodiment shown in Fig. 5B. Support for the changes in claim 20 can be found in last paragraph on page 20 of the specification. Amended claim 20 now recites the embodiment shown in Fig. 5A.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> said solar cell being disposed on a surface of said semiconductor wafer remote from said semiconductor chip.

Claim 20 calls for, inter alia:

> said solar cell being disposed areally entirely over said area of said surface of said semiconductor wafer.

The advantage of the invention of the instant application is that an operating current with a magnitude sufficient to operate the semiconductor chip during the functional test is reliably generated since the given areas for the solar cells can be increased. Moreover, due to increased solar cell area, all of the chips on the semiconductor wafer can be tested in parallel since a sufficient energy supply can be provided.

Cook et al. do not disclose such arrangements of solar cells for generating an operating current for a semiconductor chip according to the invention of the instant application. Rather, in Cook et al., the power source is located in the kerf.

Clearly, Cook et al. do not show "said solar cell being disposed on a surface of said semiconductor wafer remote from said semiconductor chip", as recited in claim 1, and "said solar cell being disposed areally entirely over said area of said surface of said semiconductor wafer", as recited in claim 20 of the instant application.

Claims 1 and 20 are, therefore, believed to be patentable over Cook et al. and since all of the dependent claims are ultimately dependent on claims 1 or 20, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1 and 7-22 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicants

YHC:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Applic. No.: 09/826,594

Marked-Up Version of the Amended Claims:

Claim 1(twice amended). A test configuration, comprising:

a semiconductor wafer;

a plurality of semiconductor chips disposed on said semiconductor wafer, each of said plurality of semiconductor chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source [for providing an electrical energy supply from energy fed in contactlessly, said energy source] disposed on said semiconductor wafer and connected to said semiconductor chip for providing [the] an electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly[;

said semiconductor wafer having a scribe line for separating said plurality of semiconductor chips from one another, and said solar cell being disposed in said scribe line], said solar cell being disposed on a surface of said semiconductor wafer remote from said semiconductor chip;

said semiconductor wafer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip, at a boundary between said plated-through hole and said semiconductor wafer, and said semiconductor wafer having a pn junction disposed along said plated-through hole for preventing a current flow between said plated-through hole and a remainder of said semiconductor wafer.

Claim 7(amended). The test configuration according to claim [4] 20, including a radiation-absorbing layer disposed between said solar cell and said semiconductor chip.

Claim 20(amended). A test configuration, comprising:

a semiconductor wafer having a surface with an area;

a plurality of semiconductor [chip] chips disposed on said surface of said semiconductor wafer, each of said semiconductor [chip] chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source [for providing an electrical energy supply from energy fed in contactlessly, said energy source] disposed

[on] above said semiconductor wafer and connected to said semiconductor chip for providing [the] an electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly, said solar cell being disposed areally [on a] entirely over said area of said surface of said semiconductor wafer.